In the United States Patent and Trademark Office

In re the Application of
Lee D. Whetsel

Divisional of Appln No: ~~10/469,274~~ 10/689,374 64

Filed: herewith

TI-14124D.4

Previous Art Unit: 2131

Previous Examiner: Hua, Ly

Title: Digital Bus Monitor Integrated Circuits

Petition to Make Special
Under 37 CFR 1.102 and
MPEP section 708.02, Paragraph VIII

October 20, 2003

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as Express Mail airbill EV333320867US in an envelope addressed to: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 20, 2003.

Lawrence J. Bassuk, Reg. No. 29,043

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Petition With Fee

Applicant submits this petition to make special accompanied by the fee set forth in 37 CFR 1.17(h).

Please charge the fee under 37 CFR 1.17(h) of $130.00 to the deposit account of Texas Instruments Incorporated, Account No.20-0668.

Claims Directed To Single Invention

The accompanying Preliminary Amendment A presents claims directed to a single invention.

Statement of Pre-Examination Search Performed

Applicant submits a copy of two pre-examination search report letters, dated September 22, 2003 and October 2, 2003, from an Arlington, Virginia search firm.

Each report letter lists the subject matter of the search, lists the field of search, and states that the subclasses for searching were confirmed by an examiner.

Submission of Most Closely Related References

Each search report letter lists the art located in that search.

The electronically filed Information Disclosure Statement A (IDS-A) and accompanying PTO-1449 forms list US patents and US Patent Application Publications located in the pre-examination searches. The electronically filed IDS-A papers also list US patents of the present named inventor, and US patents and US Patent Application Publications cited in corresponding and other patent applications of the present named inventor. Under the new rules, applicant does not submit any copies of the US patents or US Patent Application Publications cited in the electronically filed IDS-A.

An enclosed paper IDS-A and PTO-1449 forms list Foreign Patent Documents and Other Documents cited in corresponding and other patent applications of the present named inventor; applicant encloses a copy of each listed reference.

Detailed Discussion of References Cited in Search Report Letters

Applicant relies upon the combination of all the limitations in the independent claims for patentability and not any general description.

Independent claims 25, 39, and 53 distinguish over the cited art by requiring: a serial data or scan signal input lead; a serial data or scan signal output lead; a serial scan path coupled between the serial input lead and the serial output lead; a protocol selection memory coupled to the serial scan path; and an event control circuit coupled to the protocol selection memory.

The cited art fails to disclose a protocol selection memory coupled to a serial scan path, in the defined combinations.

Applicant could repeat a statement of these distinguishing limitations after the discussion of each following cited patent to meet the requirements of 37 CFR 1.111(b) and (c). Since each cited patent and the cited patents in combination fail to teach or suggest these distinguishing limitations, applicant will rely upon the preceding statement of the distinguishing limitations, without repetition.

US Patents

US 3,633,100 to Heilweil, et al., discloses applying two binary levels and an intermediate level of inputs to binary logic under test and to simulation logic. The outputs of the circuit under test and the simulation logic are compared to ascertain a good circuit.

US 3,657,527 to Kassabgi, et al., discloses a system for automatically checking boards bearing integrated circuits. A program card is read automatically to provide both test input signals to the board and simulation output signals representative of the correct output signals.

US 3,826,909 to Ivashin discloses a binary counter applying identical signals to a tested and standard reference circuit. Output indicators display any difference between the tested and standard reference circuit.

US 4,433,413 to Fasang discloses a microprocessor system including a pseudo-random pattern generator, a signature register, supplemental control logic, serial and parallel I/O port test logic, and an LED display. Test instructions and the pattern generator provide test input data. The signature register and the microprocessor process the test results and present them on the display.

US 4,439,858 to Petersen discloses a digital in-circuit tester for high speed computer control in obtaining high pulse fidelity at each electrical node of a circuit under test. The tester includes a plurality of programmed memory digital test-signal generators responsive to the computer for generating and supplying to the nodes of the circuit under test a complex sequence of digital logic signals. High pulse fidelity is obtained by minimizing the current in the power supply and digital test signal loops.

US 4,441,075 to McMahon discloses the testing of individual chips and interchip connections on or within a high density

packaging structure without a precision probe using Level Sensitive Scan Design rules.

US 4,494,066 to Goel, et al. discloses chips in a module or any second level package. The test mechanism built into each chip will be used in place of mechanical probes to perform a chip-in-place test and interchip wiring test of the package. Level sensitive scan design rules need to be used for each chip and for the package clock distribution network. Corresponds to US 4,441,075 and 4,504,784. US 4,504,784 was cited in parent patent US 5,905,738.

US 4,642,561 to Groves, et al., discloses compressing the amount of data stored in local test data RAMs for implementing a circuit test.

US 4,646,299 to Schinabeck, et al. discloses applying static analog voltages or currents to pins of a device under test and measuring resulting currents or voltages to evaluate the responses of the device being tested.

US 4,683,569 to Rubin discloses connecting test points to shift registers that are read out bidirectionally. The data in the shift registers is shifted in each direction and compared to a reference data signal to indicate an error in a test point.

US 4,701,921 to Powell, et al. discloses a modularized scan path for serially tested logic. Modules 26 each have serial registers 34-40, input gate 48 and output gate 50. Address 16 and control 12 leads connect to address decode/select 52, which selectively connects the scan data in leads 28 and the scan data

out leads 30 to the modules for testing. Corresponds to US 4,710,931 and US 4,710,933.

US 4,710,932 to Hiroshi discloses comparing cross correlation values from a device under test and a reference device where the values from both devices are counted with no delay and with delays made in steps to a predetermined time interval.

US 4,752,929 to Kantz, et al. discloses testing a semiconductor memory part by subdividing the memory array into cell fields and comparing data bits in corresponding storage cells of each field.

US 4,857,835 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application and it issued on August 15, 1989. The present application claims priority to an application filed on June 30, 1989. In any event, IDS-A, Attachment A includes comments to this patent.

US 4,860,290 to Daniels, et al. discloses a logic circuit having individually testable logic modules. Each of the modules may be selected for testing by means of a scan path in the module made up of serial register latches (SRLs) 34. Each module has a test port 28a.

US 4,872,169 to Whetsel discloses a hierarchical scan selection system. A serial scan path can be compressed or expanded to pass only through the desired logic element(s) to be tested. Corresponds to JP 63-308,583.

US 4,897,842 to Herz, et al. discloses a signature generator connected to plural circuit nodes to be tested.

US 4,907,230 to Heller, et al. discloses a device comparing the digital or analog outputs of circuit boards or other units under test with known good models. A clip connects each point of the circuit under test to a pin of the test instrumentation.

US 4,924,468 to Horak, et al. discloses a logic analyzer measuring signals that are delivered by a number of targets, such as microprocessors, that are not correlated in time.

US 4,929,889 to Seiler, et al. discloses a test/load bus internal to an integrated circuit to supply test data to test nodes internal of the chip and unload response data from the test nodes. This patent was cited in parent patents, US 5,905,738 and US 6,131,171.

US 4,931,723 to Jeffrey, et al. discloses a test device having plural tester channels. Each channel has a channel control circuit means coupled to a pin of a unit under test for controlling the state of operation of the pin.

US 5,001,713 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application and it issued on March 19, 1991. The present application claims priority to an application filed on June 30, 1989. In any event, IDS-A, Attachment A includes comments to this patent.

US 5,051,996 to Bergeson, et al. discloses a built-in test by signature system that provides fault detection by the bits in the signature detection logic.

US 5,054,024 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application and the application was filed on August 9, 1989. The present application claims priority to an application filed on June 30, 1989. In any event, IDS-A, Attachment A includes comments to this patent.

US 5,109,383 to Chujo discloses scan path latch circuits. The latch circuits include three switches and two flip-flops

US 5,161,160 to Yaguchi, et al. discloses scan paths SP100-SP107 connected to different bus lines IB0-IB7, respectively.

Foreign Patents

EP 315,475 A2 has the same disclosure as and claims priority from US 4,857,835, described above.

Conclusion

The cited references, alone or in combination, fail to teach or suggest the claimed inventions. The application is in allowable form. Applicant respectfully requests allowance of the application.

Respectfully submitted,

Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5458

D.4

PatPro
PATENT AND TRADEMARK PROFESSIONAL SERVICES
Suite 309A
Crystal Plaza One
2001 Jefferson Davis Highway
Arlington, VA 22202
703-412-4866 phone
703-412-4884 fax
www.e-pat.com

October 2, 2003

VIA FEDEX

Frank D. Cimino, Esq.
TEXAS INSTRUMENTS
7839 Churchill Way
Mail Station 3999
Dallas, TX 75251

RE: PROTOCOL APPARATUS WITH EVENT INPUT LEAD
Your Ref. No.: T1-4124D
Our Docket/Invoice No.: 30915.TI

Dear Frank:

In response to your letter dated September 18, 2003, we performed the patentability search, which you requested. The following is a complete report of our search parameters and findings.

SUBJECT MATTER OF SEARCH

In our search, we looked for specific limitations in concert with those embodied by the claims of your submitted disclosure. In particular, we looked for an integrated circuit that comprises of functional circuits, a serial data input lead, a serial data output lead, serial scan path of scan registers, a protocol selection memory, an event circuit, an access port and a comparator circuit. Note that our search was limited to finding relevant US patents and foreign publications prior to June 30, 1989.

REFERENCES DISCOVERED

5,054,024	Whetsel
5,001,713	Whetsel
4,642,561	Groves et al.
4,897,842	Herz et al.
5,109,383	Chujo

5,161,160	Yaguchi et al.
5,051,996	Bergeson et al.
4,929,889	Seiler et al.
4,907,230	Heller et al.
4,872,169	Whetsel, Jr.
4,857,835	Whetsel, Jr.
4,710,932	Hiroshi
4,752,929	Kantz et al.
4,494,066	Goel et al.
4,441,075	McMahon
3,826,909	Ivashin
3,657,527	Kassabgi et al.
3,633,100	Hellwell et al.

DISCUSSION OF REFERENCES

Whetsel *024 discloses a system scan path architecture (See Figures and Claims).

Whetsel *713 disclose an event qualified testing system and apparatus (See Figures and Claims).

Groves et al. disclose a circuit tester having on-the-fly comparison of actual and expected signals on test pins (See Figures and Abstract).

Herz et al. disclose an integrated circuit signature analyzer system having generator means integrated with the circuits to be tested, connecting means that connect the generator means to receive binary signals from a plurality of nodes in the digital circuit and comparator and storage means for receiving, storing and comparing consecutively-generated signature words (See Claims).

Chujo discloses a scan path circuit (See Figures and Abstract).

The remaining references are cited as of general interest for your review.

FIELD OF SEARCH

CLASS	SUBCLASS
714	25, 27, 30, 31, 37, 47, 724, 726, 727, 729, 731, 732, 733, 734, 735, 736, 744, For. 100, For. 300

In addition to a complete search of the above subclasses, Primary Examiner Stephen Baker of Group 2100 was consulted. This Examiner confirmed our opinion that the most pertinent search areas were covered by the above subclasses.

Enclosed are copies of the cited references and our invoice for services rendered and disbursements for this matter.

In closing, we would like to thank-you for giving us this opportunity to serve you. If there are any questions or comments concerning this search or our services, please contact us at your earliest convenience.

Sincerely,

Tuan Nguyen

In The "Received" stamp of the Patent and Trademark Office imprinted hereon acknowledges the filing of:

___ NEW APPLICATION.	_x_ AMENDMENT A - preliminary – 1.111
_x_ DECLARATION (copy)	___ EOT
___ ASSIGNMENT	___ NOTICE OF APPEAL
_x_ FORMAL DRAWINGS (6 sheets)	___ APPEAL
___ INFORMAL DRAWINGS	_x_ Petition to Make Special
___ CONTINUATION APP'N	_x_ Divisional fee transmittal
_x_ DIVISIONAL APP'N	_x_ IDS A & Form 1449A

NAME OF INVENTOR(S): Lee D Whetsel	RECEIPT DATE & SERIAL NO.: **Serial No.:**
TITLE OF INVENTION: Digital Bus Monitor Integrated Circuits	
TI FILE NO.: TI-14124D.4 / DEPOSIT ACCT NO.: **20-0668**	
EXPRESS MAIL RCPT NO.: EV333320867US MLD: October 20, 2003 DUE: ATTY/SEC'Y: LJB/sg	

22582 U.S. PTO
10/689374

102003

RECEIVED
OCT 3 1 2003
PATENT DEPT

TEXAS INSTRUMENTS

FAX COVER SHEET

DATE: July 28, 2004

FROM: Lawrence J. Bassuk	**TO: Examiner Clayton La Balle**
COMPANY NAME:	**COMPANY NAME: USPTO**
TEXAS INSTRUMENTS INCORPORATED	**PHONE NUMBER: 571-272-1594**
PHONE NUMBER: 972/917-5458	**FAX NUMBER: 571-273-1594**
FAX NUMBER: 972/917-4418	

MESSAGE

RE: S.N. 10/689,374
TI-14124D.4

Copies of filed documents to follow.

Fax sent by: Shannon Gragsone

Texas Instruments Incorporated - Post Office Box 655474- Dallas, Texas 75265
7839 Churchill Way, -Dallas -972-917-5460-FAX # 972-917-4418

PatPro
PATENT AND TRADEMARK PROFESSIONAL SERVICES
Suite 309A
Crystal Plaza One
2001 Jefferson Davis Highway
Arlington, VA 22202
703-412-4866 phone
703-412-4884 fax
www.e-pat.com

OFFICIAL

September 22, 2003

VIA FEDEX

Frank D. Cimino, Esq.
TEXAS INSTRUMENTS
7839 Churchill Way
Mail Station 3999
Dallas, TX 75251

RE: EVENT INPUT PINS
Your Ref. No.: T14124D.x
Our Docket/Invoice No.: 30892.TI

Dear Frank:

In response to your letter dated September 11, 2003, we performed the patentability search, which you requested. The following is a complete report of our search parameters and findings.

SUBJECT MATTER OF SEARCH

In our search, we looked for specific limitations in concert with those embodied by the claims of your submitted disclosure. In particular, we searched for an integrated circuit that comprises of a substrate, operating circuits, a serial data input lead, a serial data output lead, a mode select signal input lead, comparator circuits, event circuits a command register, a data register, and an access port, all formed on the substrate. Note that our search was limited to finding relevant US patents and foreign publications prior to June 30, 1989.

REFERENCES DISCOVERED

4,857,835	Whetsel, Jr.
5,001,713	Whetsel
4,433,413	Fasang
5,051,996	Bergeson et al.
4,931,723	Jeffery et al.
4,924,468	Horak et al.

4,872,169	Whetsel, Jr.
4,860,290	Daniels et al.
4,701,921	Powell et al.
4,683,569	Rubin
4,646,299	Schinabeck et al.
4,642,561	Groves et al.
4,439,858	Petersen
3,826,909	Ivashin
3,657,527	Kassabgi et al.
3,633,100	Hellwell et al.
EP315475A2	Whetsel, Jr.

DISCUSSION OF REFERENCES

Whetsel, Jr. discloses a global event qualification system for integrated circuits (See Claims).

Whetsel discloses an event qualified testing architecture for integrated circuits, which includes input circuitry, output circuitry, application logic circuitry and test circuitry (See Figures and Claims).

Fasang discloses a built-in apparatus and method for testing a microprocessor system, which includes memory means, data source means, signature register means and comparator means (See Figures and Claim 1).

The remaining references are cited as of general interest for your review.

FIELD OF SEARCH

CLASS	SUBCLASS
714	25, 26, 27, 30, 31, 37, 44, 724, 726, 727, 729, 730, 731, 732, 733, 734, 736, 744, For. 100, For. 293, For. 300

In addition to a complete search of the above subclasses, Primary Examiner Cynthia Britt of Group 2100 was consulted. This Examiner confirmed our opinion that the most pertinent search areas were covered by the above subclasses.

Enclosed are copies of the cited references and our invoice for services rendered and disbursements for this matter.

In closing, we would like to thank-you for giving us this opportunity to serve you. If there are any questions or comments concerning this search or our services, please contact us at your earliest convenience.

Sincerely,

Tuan Nguyen